AMENDMENTS TO THE CLAIMS

A detailed listing of all claims that are, or were, in the present application, irrespective of whether the claim(s) remains under examination in the application are presented below. The claims are presented in ascending order and each includes one status identifier. Those claims not cancelled or withdrawn but amended by the current amendment utilize the following notations for amendment: 1. deleted matter is shown by strikethrough for six or more characters and double brackets for five or less characters; and 2. added matter is shown by underlining.

1-72. (Cancelled).

73. (Previously Presented) An insulating substrate board for a semiconductor comprising:

a ceramic substrate board; and

a metal alloy layer consisting essentially of aluminum of not less than 98% by weight and of silicon of not less than 0.2% by weight and not more than 0.5% by weight,

wherein the metal alloy layer is bonded on at least one surface portion of the ceramic substrate board, and wherein a Vickers hardness of the metal alloy layer is not less than 25 and not more than 35.

74. (Previously Presented) The insulating substrate board according to claim 73, wherein the metal alloy layer is bonded on at least one surface portion of the ceramic substrate board by direct bonding.

75. (Previously Presented) The insulating substrate board according to claim 73, wherein the metal alloy layer is bonded on at least one surface portion of the ceramic substrate board through a brazing material layer.

76. (Previously Presented) An insulating substrate board for a semiconductor comprising:

a ceramic substrate board; and

a metal alloy layer consisting essentially of aluminum, silicon of about 0.6% by weight, and Mn of about 1.5% by weight,

wherein the metal alloy layer is bonded by direct bonding on at least one surface portion of the ceramic substrate board, and wherein a Vickers hardness of the metal alloy layer is not less than 25 and not more than 35.

77. (Previously Presented) An insulating substrate board for a semiconductor comprising:

a ceramic substrate board; and

a metal alloy layer consisting essentially of aluminum, silicon of not less than 0.1% by weight and not more than 0.4% by weight, and Mg of not less than 0.5% by weight and not more than 1% by weight,

wherein the metal alloy layer is bonded on at least one surface portion of the ceramic substrate board, and wherein a Vickers hardness of the metal alloy layer is not less than 25 and not more than 35.

78. (Previously Presented) The insulating substrate board according to claim 77, wherein the metal alloy layer is bonded on at least one surface portion of the ceramic substrate board by direct bonding.

79. (Previously Presented) The insulating substrate board according to claim 77, wherein the metal alloy layer is bonded on at least one surface portion of the ceramic substrate board through a brazing material layer.

80-82. (Cancelled)

83. (Previously Presented) An insulating substrate board for a semiconductor comprising:

a ceramic substrate board; and

a metal alloy layer consisting essentially of aluminum and of Cu of not less than 1.0% by weight and not more than 2.0% by weight,

wherein the metal alloy layer is bonded on at least one surface portion of the ceramic substrate board, and wherein a Vickers hardness of the metal alloy layer is not less than 25 and not more than 35.

84. (Previously Presented) The insulating substrate board according to claim 83, wherein the metal alloy layer is bonded on at least one surface portion of the ceramic substrate board by direct bonding.

85. (Previously Presented) The insulating substrate board according to claim 83, wherein the metal alloy layer is bonded on at least one surface portion of the ceramic substrate board through a brazing material layer.

86. (Previously Presented) An insulating substrate board for a semiconductor comprising:

a ceramic substrate board; and

a metal alloy layer consisting essentially of aluminum and of Zn of about 2.0% by weight,

wherein the metal alloy layer is bonded on at least one surface portion of the ceramic substrate board, and wherein a Vickers hardness of the metal alloy layer is not less than 25 and not more than 35.

87. (Previously Presented) The insulating substrate board according to claim 86, wherein the metal alloy layer is bonded on at least one surface portion of the ceramic substrate board by direct bonding.

88. (Previously Presented) The insulating substrate board according to claim 86, wherein the metal alloy layer is bonded on at least one surface portion of the ceramic substrate board through a brazing material layer.

89-92. (Cancelled)

93. (Previously Presented) An insulating substrate board for a semiconductor comprising:

a ceramic substrate board; and

a metal alloy layer consisting essentially of aluminum, silicon of about 0.1% by weight, and Cu of about 1.0% by weight,

wherein the metal alloy layer is bonded on at least one surface portion of the ceramic substrate board, and wherein a Vickers hardness of the metal alloy layer is not less than 25 and not more than 35.

94. (Previously Presented) The insulating substrate board according to claim 93, wherein the metal alloy layer is bonded on at least one surface portion of the ceramic substrate board by direct bonding.

95. (Previously Presented) The insulating substrate board according to claim 93, wherein the metal alloy layer is bonded on at least one surface portion of the ceramic substrate board through a brazing material layer.

96. (Previously Presented) An insulating substrate board for a semiconductor comprising:

a ceramic substrate board; and

a metal alloy layer consisting essentially of aluminum, Si of about 0.1% by weight, Cu of about 1.0% by weight, and Mg of about 0.1% by weight,

wherein the metal alloy layer is bonded on at least one surface portion of the ceramic substrate board, and wherein a Vickers hardness of the metal alloy layer is not less than 25 and not more than 35.

97. (Previously Presented) The insulating substrate board according to claim 96, wherein the metal alloy layer is bonded on at least one surface portion of the ceramic substrate board by direct bonding.

98. (Previously Presented) The insulating substrate board according to claim 96, wherein the metal alloy layer is bonded on at least one surface portion of the ceramic substrate board through a brazing material layer.

99. (Previously Presented) A power module comprising:

a ceramic substrate board;

metal alloy layers consisting essentially of aluminum of not less than 98% by weight and of silicon of not less than 0.2% by weight and not more than 0.5% by weight, wherein the metal alloy layers are bonded on both surfaces of the ceramic substrate board;

a metal base plate bonded to one of the metal alloy layers; and

a semiconductor tip formed on the other of the metal alloy layer,

wherein a Vickers hardness of the metal alloy layer is not less than 25 and not more than 35.

100. (Previously Presented) The power module according to claim 99, wherein the metal alloy layers are bonded on the ceramic substrate board by direct bonding.

101. (Previously Presented) The power module according to claim 99, wherein the metal alloy layers are bonded on the ceramic substrate board through a brazing material layer.

102. (Previously Presented) A power module comprising:

a ceramic substrate board;

metal alloy layers consisting essentially of aluminum, silicon of about 0.6% by weight, and Mn of about 1.5% by weight, wherein the metal alloy layers are bonded on both surfaces of the ceramic substrate board;

a metal base plate bonded to one of the metal alloy layers; and

a semiconductor tip formed on the other of the metal alloy layer,

wherein a Vickers hardness of the metal alloy layer is not less than 25 and not more than 35.

103. (Previously Presented) A power module comprising:

a ceramic substrate board;

metal alloy layers consisting essentially of aluminum, silicon of not less than 0.1% by weight and not more than 0.4% by weight, and Mg of not less than 0.5% by weight and not more than 1% by weight, wherein the metal alloy layers are bonded on both surfaces of the ceramic substrate board;

a metal base plate bonded to one of the metal alloy layers; and

a semiconductor tip formed on the other of the metal alloy layer,

wherein a Vickers hardness of the metal alloy layer is not less than 25 and not more than 35.

104. (Previously Presented) The power module according to claim 103, wherein the metal alloy layers are bonded on the ceramic substrate board by direct bonding.

105. (Previously Presented) The power module according to claim 103, wherein the metal alloy layers are bonded on the ceramic substrate board through a brazing material layer.

106-108. (Cancelled).

109. (Previously Presented) A power module comprising:

a ceramic substrate board;

metal alloy layers consisting essentially of aluminum and of Cu of not less than 1.0% by weight and not more than 2.0% by weight, wherein the metal alloy layers are bonded on both surfaces of the ceramic substrate board;

a metal base plate bonded to one of the metal alloy layers; and

a semiconductor tip formed on the other of the metal alloy layer,

wherein a Vickers hardness of the metal alloy layer is not less than 25 and not more than 35.

110. (Previously Presented) The power module according to claim 109, wherein the metal alloy layers are bonded on the ceramic substrate board by direct bonding.

111. (Previously Presented) The power module according to claim 109, wherein the metal alloy layers are bonded on the ceramic substrate board through a brazing material layer.

112. (Previously Presented) A power module comprising:

a ceramic substrate board;

metal alloy layers consisting essentially of aluminum and of Zn of about 2.0% by weight, wherein the metal alloy layers are bonded on both surfaces of the ceramic substrate board;

a metal base plate bonded to one of the metal alloy layers; and

a semiconductor tip formed on the other of the metal alloy layer,

wherein a Vickers hardness of the metal alloy layer is not less than 25 and not more than 35.

113. (Previously Presented) The power module according to claim 112, wherein the metal alloy layers are bonded on the ceramic substrate board by direct bonding.

114. (Previously Presented) The power module according to claim 112, wherein the metal alloy layers are bonded on the ceramic substrate board through a brazing material layer.

115-118. (Cancelled).

119. (Previously Presented) A power module comprising:

a ceramic substrate board;

metal alloy layers consisting essentially of aluminum, silicon of about 0.1% by weight, and Cu of about 1.0% by weight, wherein the metal alloy layers are bonded on both surfaces of the ceramic substrate board;

a metal base plate bonded to one of the metal alloy layers; and

a semiconductor tip formed on the other of the metal alloy layer,

wherein a Vickers hardness of the metal alloy layer is not less than 25 and not more than 35.

120. (Previously Presented) The power module according to claim 119, wherein the metal alloy layers are bonded on the ceramic substrate board by direct bonding.

121. (Previously Presented) The power module according to claim 119, wherein the metal alloy layers are bonded on the ceramic substrate board through a brazing material layer.

122. (Previously Presented) A power module comprising:

a ceramic substrate board;

metal alloy layers consisting essentially of aluminum, Si of about 0.1% by weight, Cu of about 1.0% by weight, and Mg of about 0.1% by weight, wherein the metal alloy layers are bonded on both surfaces of the ceramic substrate board;

a metal base plate bonded to one of the metal alloy layers; and

a semiconductor tip formed on the other of the metal alloy layer,

wherein a Vickers hardness of the metal alloy layer is not less than 25 and not more than 35.

123. (Previously Presented) The power module according to claim 122, wherein the metal alloy layers are bonded on the ceramic substrate board by direct bonding.

124. (Previously Presented) The power module according to claim 123, wherein the metal alloy layers are bonded on the ceramic substrate board through a brazing material layer.